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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,105	MONTHIE ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/696,105 filed on 10/29/2003. Claims 1 – 20 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 3, before "steps" delete —**the**—.
Claim 4, line 3, change "proper" to —**property**—.
Claim 5, line 2, before "step" delete —**the**—.
Claim 6, line 1, after "wherein" insert —**said**—.
Claim 6, line 2, before "alternative" delete —**said**—.
Claim 7, line 1, after "wherein" insert —**said**—.
Claim 7, line 2, before "alternative" delete —**said**—.
Claim 10, line 1, after "wherein" insert —**said**—.
Claim 10, line 2, before "alternative" delete —**said**—.
Claim 11, line 1, change "generating" to —**providing**—.
Claim 11, line 2, before "step" delete —**the**—.
Claim 13, line 2, before "step" delete —**the**—.
Claim 14, line 2, before "step" delete —**the**—.
Claim 15, line 2, before "step" delete —**the**—.
Claim 19, line 3, change "block" to —**of said one or more blocks**—.
Claim 20, line 2, change "block" to —**of said one or more blocks**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,696,943 to *Dennis Lee* in view of U.S. Patent No. 6,453,454 B1 to *Kuochun Lee et al.*

5. As to Claim 1, *Dennis Lee* shows and discloses the following subject matter:

- *IP blocks* (e.g., A/D converter section 304, TAI section 308 etc.) and a plurality of *spare gates sets (i.e., spare cells) 402, 406* in a wireless *LAN product 300* (i.e., *structured ASIC*) – [Fig. 3; Fig. 4; Fig. 2; col. 5, line 52 – col. 6, line 14];
- *Spare cells* are made of *standard cell gates* – [col. 3, line 19 – 26; Fig. 2];
- Effective *design and/or layout modifications* of *IP blocks* of an existing wireless LAN product using spare cells (i.e., cell-based building blocks) – [col. 4, line 35 – col. 5, line 4]

Notice that IP blocks, which are semiconductor devices, are constructed (i.e., implemented) using a plurality of standard cell gates (cell-based building blocks). *Dennis Lee* teaches using spare cells (cell-based building blocks) in design and/or layout modifications of a IP block in a semiconductor device (wireless LAN), he does not teach providing one or more alternative views of a IP block using the spare cells (cell-based building blocks). But *Kuochun Lee et al.* teach automatic ECO (engineering change order) methodology which uses spared gate array cells (i.e., cell-based building blocks) to change physical layout through ECO modifications thereby providing one or more alternative views of an existing logic circuit design (e.g., IP block) – [title; abstract].

Kuochun Lee et al. also teach that utilizing spared gate array cells in ECO modifications can significantly reduce turn-around time of a new design – [col. 4, line 31 – 60].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Kuochun Lee et al.* in utilizing spared gate array cells (cell-based building blocks) and automatic ECO methodology in change physical layout through ECO modifications thereby quickly providing one or more alternative views of one or more IP blocks in redesign and upgrade of an existing ASIC device.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 16, reasons are included in **[Response A]** given above. Notice that the ECO modification can be applied to modify a default view (e.g., physical layout) of a IP block.

7. As to Claim 18, in addition to reasons included in **[Response A]** given above, *Kuochun Lee et al.* teaches the following subject matter:

- ECO modifications of physical layout of an integrated circuit comprising *base layers* and *metal layers* – [col. 10, line 33 – 60];
- Updated physical layout retains essentially all of the original physical layout's base layer(s)...metal layer(s) includes connections that must be made to selected spared gate array cells to implement the required ECO changes – [col. 5, line 51 – 56].

For reference purposes, the explanations given above in response to Claim 18 are called **[Response B]** hereinafter.

8. As to Claim 2, reasons are included in **[Response A]** given above. Notice that the cell-based building blocks can be made of spare cells, which are standard cell gates.

9. As to Claim 3, *Dennis Lee* shows and discloses the subject matter in [Fig. 2; col. 5, line 26 – 33].

10. As to Claim 4, *Kuochun Lee et al.* and *Dennis Lee* teaches the following subject matter:

- ECO modifications of physical layout of an integrated circuit comprising *base layers* and *metal layers* – [*Kuochun Lee et al.*; col. 10, line 33 – 60];
- Updated physical layout retains essentially all of the original physical layout's base layer(s)...metal layer(s) includes connections that must be made to selected spared gate array cells to implement the required ECO changes – [*Kuochun Lee et al.*; col. 5, line 51 – 56].
- Spare cell gates (standard cell gates) are placed in proper locations – [*Dennis Lee*; col. 4, line 45 – 51]; Spare cell gates are placed at fixed locations close to one or more IP blocks – [*Dennis Lee*; Fig. 4].

11. As to Claim 5, *Kuochun Lee et al.* teach the following subject matter:

- Spare gate array cells reserved for ECO modifications of a design (e.g., IP block) – [col. 3, line 39 – 67];
- Gate array database includes information regarding spare gate array cells available for ECO modifications...information includes physical locations, timing information, fanout characteristics – [col. 6, line 27 – 53].

Notice that, for future ECO modifications due to speed, fanout etc., one or more alternative views of physical layout of an IP block are generated.

12. As to Claims 6 – 8, *Kuochun Lee et al.* show in Fig. 4 and teach that spare gate array cells can be *manually* and/or *automatically* selected in generating an alternative view of an IP block through ECO modifications. Notice that the automatic ECO methodology performs ECO changes by modifying programs embedded in a CAD tool using a text editor.

13. As to Claim 9, *Kuochun Lee et al.* show and teach the subject matter in Fig. 1. Notice that an alternative view of an IP block and be generated by a ECO HDL specification 107 using ECO compiler 108. RTL is a HDL.

14. As to Claim 10, *Kuochun Lee et al.* show in Fig. 1 and teach that an alternative view of a IP block is stored in an ECO netlist 109, it is generated prior to instantiation (i.e., without metal layer connection/routing of spare gate array cells).

15. As to Claims 11, 17 and 19, *Kuochun Lee et al.* show in Fig. 4 and teach updating ECO netlist file 406.

16. As to Claims 12 and 20, *Dennis Lee* shows in Fig. 2 and teaches that unused (i.e., spare) building blocks are tied off.

17. As to Claims 13 – 15, *Kuochun Lee et al.* show and teach the following subject matter:

- ECO synthesis to maximally *reuse old logic* during resynthesis, and *spare cell mapping* to map new logic functions onto reserved spared standard cells – [col. 2, line 35 – 52];
- Generation of *physical layout (view)* (of modified IP block) in ECO to document desired changes – [col. 2, line 15 – 20; Fig. 1; Fig. 3; Fig. 4];
- Routing (modified) IP block based on modified (ECO) netlist – [Fig. 1; Fig. 3; Fig. 4].

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
October 12, 2005